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10/036,323	12/31/2001	Philip L. Hower	TI-30010	3224

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EXAMINER
DICKEY, THOMAS L

ART UNIT	PAPER NUMBER
2826	

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8

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/036,323	Applicant(s) HOWER ET AL.	
	Examiner Thomas L Dickey	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on *04 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *27-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-26* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group II claims 1-26 in Paper No. 7 is acknowledged.

Oath/Declaration

2. The oath/declaration filed on 04/05/02 is acceptable.

Drawings

3. The formal drawings filed on 04/05/02 are approved as to form. In accordance with applicant's instruction of 04/05/02, original sheets filed 12/31/01 have been cancelled. A form 948 indicating draftsman's approval of the 04/05/02 drawings is attached.

As to substance, the drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the combination of all four of these distinctly claimed (note claim 14) parts:

1. source metallization
2. a p-type surface body diffusion
3. a p-type buried body diffusion

4. an ohmic connection between said buried body diffusion and said source metallization

as well as their claimed relationships to each other and to other claimed elements, must be shown or the feature(s) canceled from the claim(s). Furthermore, the "further p+ diffusion" and the "aperture" in the gate structure of claim 15 must be shown or these features cancelled. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Priority

4. Acknowledgement is made of applicant's claim for domestic priority under 35 U.S.C. 119(e), through provisional application 60/259,322 filed 12/31/00.

Information Disclosure Statement

5. If applicant is aware of any relevant prior art, he/she requested to cite it on form **PTO-1449** in accordance with the guidelines set forth in M.P.E.P. 609.

The listing of a reference on page 6 line 11 in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be

submitted in a separate paper." Therefore, unless the examiner has cited the reference on a form PTO-892, it has not been considered.

Specification

6. The disclosure is objected to because of the following informalities:

The incorporation of essential material in the specification by reference to a publication, as attempted on page 6 of the instant application, is improper. Applicants are required to amend the disclosure to include the material incorporated by reference. The amendment must be accompanied by an affidavit or declaration executed by the applicants, or a practitioner representing the applicants, stating that the amendatory material consists of the same material incorporated by reference in the referencing application. See *In re Hawkins*, 486 F.2d 569, 179 USPQ 157 (CCPA 1973); *In re Hawkins*, 486 F.2d 579, 179 USPQ 163 (CCPA 1973); and *In re Hawkins*, 486 F.2d 577, 179 USPQ 167 (CCPA 1973).

If on reflection applicants conclude that the Zhu and Hower papers are not essential, but merely useful background, applicants need not amend the disclosure to include the material incorporated by reference but may instead merely amend the reference to remove any inference that the Zhu and Hower material is incorporated into the specification.

Page 1 of the application contains a reference to a co-pending PCT application. Since no such application has been filed, this reference should be removed.

Further, the reference to figure 5E on page 16 line 13 should be removed, as there is no figure 5E.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 20-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 20-22 recite the limitation "said conductive body region" in each of their lines 1. There is insufficient antecedent basis for this limitation in these claims. The confusion produced by this fact cannot be removed by deduction. There are two "body regions" defined in claim 19 and both of them in fact are "conductive" although that fact is not used to name either. Further, both of the body regions to which "said conductive body region" might refer are 2nd type, while the "conductive body region" is 1st type, at least in claim 20.

The reference to "said body region," in line 5 of claim 19 may be deduced to be intended to refer to "a surface body region" in line 4, therefore claim 19 is not rejected under section 112. Nonetheless this reference should be corrected. In con-

trast, the references to "said conductive body region" in claims 20-22 make the scope of these claims unascertainable. These claims are unsearchable as written.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-5 are rejected under 35 U.S.C. 102(a) as being anticipated by EFLAND ET AL. (6,137,140).

A. With regard to claims 1 and 2, Efland et al. discloses a DMOS transistor source structure comprising: a source diffusion 11; a gate 27 which is capacitively coupled to control majority carrier flow from said source diffusion 11 through a body diffusion 24a into a semiconductor drift region; and an ohmic connection structure which is at least partly self-aligned to said body diffusion 24a, positioned to collect minority carrier flow from said drift region, and connected to divert said minority carrier flow to bypass any junction between said source 11 and body 24a diffusion, further comprising a drain region 12-23 which is laterally separated from said body diffusion 24a by said drift region. Note figure 2, column 2 lines 63-67, column 3 lines 1-32, and column 3 lines 51-61 of Efland et al.

B. Claims 3-5 are written to include two elements that invoke Section 112 paragraph 6: "means for controlling electron flow from said source diffusion into a semiconductor drift region"; and "means for collecting hole flow from said drift region, and for diverting said hole flow to bypass said source diffusion and thereby avoid secondary electron current." Analysis of these claims therefore requires that the specification be examined to determine what structure is disclosed that is capable of performing the specified functions. Upon examination of the specification, it is determined that the only disclosed structure capable of "controlling electron flow from said source diffusion into a semiconductor drift region" is the gate 24 coupled to a p-type channel region 20 shown in applicants' figures 1 and 6. It is further determined that the only disclosed structure capable of "collecting hole flow from said drift region, and for diverting said hole flow to bypass said source diffusion and thereby avoid secondary electron current" is the body 30 shown in applicants' figure 1. It is further determined that under a "function-way-means" test, Efland et al.'s gate 27 coupled to a p type channel region 24a (note figure 2 of Efland et al.) is an equivalent of applicants' gate 24 coupled to a p-type channel region 20, and that Efland et al.'s body 14 (note figure 2 of Efland et al.) is an equivalent of applicants' body 30. Therefore Efland et al. discloses a DMOS transistor source structure comprising: n-type source diffusion 11; means 27 for controlling electron flow from said source diffusion 11 into a semiconductor drift region; and means 14 for collecting hole flow from a drift region 22, and for diverting said hole flow to bypass said source diffusion 11 and thereby

avoid secondary electron current, further comprising a drain region 12-23 which is laterally separated from said means for controlling electron flow by said drift region 22, wherein said means 27 for controlling electron flow further comprises a p-type channel region (no part #, it may be seen in the body 23a, directly below gate 27) which is capacitively coupled to a conductive gate 27 structure. Note figure 2, column 2 lines 63-67, column 3 lines 1-32, and column 3 lines 51-61 of Efland et al.

Claims 6,8,10,12,14,17,19, and 23-26 are rejected under 35 U.S.C. 102(a) as being anticipated by HARRIS ET AL. (6,150,671).

A. With regard to claims 6 and 8, Harris et al. discloses a DMOS transistor source structure comprising: an n-type source diffusion 6; a p-type surface body diffusion 4 which laterally surrounds at least part of said source diffusion 6; a conductive gate structure 9 which is capacitively coupled to part of said p-type surface body diffusion 4 to define a channel region therein; and a p-type buried body diffusion 3 which diverts at least some hole current to at least partially bypass said surface body diffusion 4, wherein said buried body diffusion 3 is self-aligned to at least part of said source diffusion 6. Note figure 11, column 5 lines 23-48, and column 6 lines 30-36 of Harris et al.

B. With regard to claims 10 and 12, Harris et al. discloses a DMOS transistor source structure comprising: an n-type source diffusion 6, ohmically connected to a source metallization 11; a p-type surface body diffusion 4 which laterally surrounds at least part of said source diffusion 6, a conductive gate structure 9 which is ca-

pacitively coupled to part of said p-type surface body diffusion 4 to define a channel region therein; a p-type buried body diffusion 3 which underlies said channel and at least part of said surface body diffusion 4; and at least one additional p-type diffusion 15 component which reduces the resistance between said buried body diffusion 3 and said source metallization 11; whereby said buried body diffusion 3 diverts hole current to avoid parasitic bipolar turn-on and thereby increase the safe operating area of the device, wherein said buried body diffusion 3 is self-aligned to at least part of said source diffusion 6. Note figure 11, column 5 lines 23-48, and column 6 lines 30-36 of Harris et al.

C. With regard to claims 14 and 17, Harris et al. discloses a DMOS transistor source structure comprising: an n-type source diffusion 6, ohmically connected to a source metallization 11; a p-type surface body diffusion 4 which laterally surrounds at least part of said source diffusion 6, a conductive gate structure 9 which Is capacitively coupled to part of said p-type surface body diffusion 4 to define a channel region therein; a p-type buried body diffusion 3 which underlies said channel and at least part of said surface body diffusion 4; and an ohmic connection 15 (note that ohmic connection 15 is ohmic with source metallization 11 and is connected, albeit not directly contacting, buried body diffusion 3) between said buried body diffusion 3 and said source metallization 11; whereby said buried body diffusion 3 diverts hole current to bypass said source diffusion 6, and thereby reduces emission of secondary electrons, and thereby increases the safe operating area of the device, wherein

said buried body diffusion 3 is self-aligned to at least part of said source diffusion 6. Note figure 11, column 5 lines 23-48, and column 6 lines 30-36 of Harris et al.

D. With regard to claim 19, Harris et al. discloses a DMOS transistor source structure comprising: a first conductivity (n) type source region 6; a second conductivity (p) type surface body region 4, underlying and laterally surrounding said source region 6; a gate electrode 9 extending over at least a portion of said body region 4 to define a channel region (no part #, it is seen under gate) therein; and a drain region 7 which is part of a continuous semiconductor body with said source region 6, and which is separated from said source region 6 by at least said channel region; and a second-conductivity-type deep body region 3 underlying said source 6 and surface body 4 regions; wherein the body region 3 provides a low impedance path for holes emitted at or near said drain region 7. Note figure 11, column 5 lines 23-48, and column 6 lines 30-36 of Harris et al.

E. With regard to claims 23-26, Harris et al. discloses a DMOS transistor source structure comprising: a semiconductor layer 3-4-7; a first region 4 of a first conductivity (p) type formed in the semiconductor layer; a source region 6 of a second conductivity (n) type opposite the first region 4; a channel region defined between an edge of the source region 6 and an edge of the first region 4; a drain region 7 of the second conductivity (n) type formed in the semiconductor layer 3-4-7, the drain region 7 adjacent the channel region; a field oxide region 8 formed on the first region 4 between the source region 6 and the channel region; at least one gate 9 extending

over at least a portion of the channel region, the gate 9 formed upon a gate oxide layer 8; and a conductive body region 3 in the first region 4 and underneath the source region 6, wherein the body region 3 provides a low impedance path for holes emitted at the drain region 7, wherein said conductive body region 3 is the first conductivity (p) type and is a buried layer. Note figure 11, column 5 lines 23-48, and column 6 lines 30-36 of Harris et al. Note with regard to claim 25 only that applicant's claim does not distinguish over the Harris et al. reference regardless of the process used to form the conductive body region, because only the final product is relevant, not the recited process of high energy implanting. Note that a "product by process" claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7,9,11,13,16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over HARRIS et al. (6,150,671) in view of EFLAND et al. (6,137,140).

A. With regard to claims 7 and 9, Harris et al. discloses a DMOS transistor source structure comprising: an n-type source diffusion 6; a p-type surface body diffusion 4 which laterally surrounds at least part of said source diffusion 6; a conductive gate structure 9 which is capacitively coupled to part of said p-type surface body diffusion 4 to define a channel region therein; and a p-type buried body diffusion 3 which diverts at least some hole current to at least partially bypass said surface body diffusion 4, wherein said buried body diffusion 3 is self-aligned to at least part of said source diffusion 6. Note figure 11, column 5 lines 23-48, and column 6 lines 30-36 of Harris et al. Harris et al. does not disclose a drain region which is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor or said drain region, a/k/a drain structure which further includes at least one shallow n-well diffusion laterally surrounding an n+ drain diffusion.

However, Efland et al. discloses a drain region 12-23 which is laterally spaced from said channel by a drift region 22, to thereby define a lateral DMOS transistor and further discloses that said drain region 12-23 includes at least one shallow n-well diffusion 23 laterally surrounding an n+ drain diffusion 12. Note figure 2, column 2 lines 63-67, column 3 lines 1-32, and column 3 lines 51-61 of Efland et al. Therefore, it would have been obvious to a person having skill in the art to augment Harris et al.'s DMOS transistor source structure with the drift region including at least one shallow n-well diffusion laterally surrounding an n+ drain diffusion defining a lateral DMOS transistor such as taught by Efland et al. in order to place the advantageous features of the Harris et al. invention in the well-known lateral DMOS format to thus provide better accessibility (top-only accessibility such as may only be had with the lateral DMOS format) to the DMOS invention of Harris et al.

B. With regard to claims 11 and 13, Harris et al. discloses a DMOS transistor source structure comprising: an n-type source diffusion 6, ohmically connected to a source metallization 11; a p-type surface body diffusion 4 which laterally surrounds at least part of said source diffusion 6, a conductive gate structure 9 which is capacitively coupled to part of said p-type surface body diffusion 4 to define a channel region therein; a p-type buried body diffusion 3 which underlies said channel and at least part of said surface body diffusion 4; and at least one additional p-type diffusion 15 component which reduces the resistance between said buried body diffusion 3 and said source metallization 11; whereby said buried body diffusion 3 diverts hole

current to avoid parasitic bipolar turn-on and thereby increase the safe operating area of the device, wherein said buried body diffusion 3 is self-aligned to at least part of said source diffusion 6. Note figure 11, column 5 lines 23-48, and column 6 lines 30-36 of Harris et al. Harris et al. does not disclose a drain region which is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor or said drain region, a/k/a drain structure which further includes at least one shallow n-well diffusion laterally surrounding an n+ drain diffusion.

However, Efland et al. discloses a drain region 12-23 which is laterally spaced from said channel by a drift region 22, to thereby define a lateral DMOS transistor and further discloses that said drain region 12-23 includes at least one shallow n-well diffusion 23 laterally surrounding an n+ drain diffusion 12. Note figure 2, column 2 lines 63-67, column 3 lines 1-32, and column 3 lines 51-61 of Efland et al. Therefore, it would have been obvious to a person having skill in the art to augment Harris et al.'s DMOS transistor source structure with the drift region including at least one shallow n-well diffusion laterally surrounding an n+ drain diffusion defining a lateral DMOS transistor such as taught by Efland et al. in order to place the advantageous features of the Harris et al. invention in the well-known lateral DMOS format to thus provide better accessibility (top-only accessibility such as may only be had with the lateral DMOS format) to the DMOS invention of Harris et al.

C. With regard to claims 16 and 18, Harris et al. discloses a DMOS transistor source structure comprising: an n-type source diffusion 6, ohmically connected to a

source metallization 11; a p-type surface body diffusion 4 which laterally surrounds at least part of said source diffusion 6, a conductive gate structure 9 which Is capacitively coupled to part of said p-type surface body diffusion 4 to define a channel region therein; a p-type buried body diffusion 3 which underlies said channel and at least part of said surface body diffusion 4; and an ohmic connection 15 (note that ohmic connection 15 is ohmic with source metallization 11 and is connected, albeit not directly contacting, buried body diffusion 3) between said buried body diffusion 3 and said source metallization 11; whereby said buried body diffusion 3 diverts hole current to bypass said source diffusion 6, and thereby reduces emission of secondary electrons, and thereby increases the safe operating area of the device, wherein said buried body diffusion 3 is self-aligned to at least part of said source diffusion 6. Note figure 11, column 5 lines 23-48, and column 6 lines 30-36 of Harris et al. Harris et al. does not disclose a drain region which is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor or said drain region, a/k/a drain structure which further includes at least one shallow n-well diffusion laterally surrounding an n+ drain diffusion.

However, Efland et al. discloses a drain region 12-23 which is laterally spaced from said channel by a drift region 22, to thereby define a lateral DMOS transistor and further discloses that said drain region 12-23 includes at least one shallow n-well diffusion 23 laterally surrounding an n+ drain diffusion 12. Note figure 2, column 2 lines 63-67, column 3 lines 1-32, and column 3 lines 51-61 of Efland et al.

Therefore, it would have been obvious to a person having skill in the art to augment Harris et al.'s DMOS transistor source structure with the drift region including at least one shallow n-well diffusion laterally surrounding an n+ drain diffusion defining a lateral DMOS transistor such as taught by Efland et al. in order to place the advantageous features of the Harris et al. invention in the well-known lateral DMOS format to thus provide better accessibility (top-only accessibility such as may only be had with the lateral DMOS format) to the DMOS invention of Harris et al.

Allowable Subject Matter

Claim 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. This claim is considered allowable over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a combination including at least four distinct elements in the body, namely, a p-type surface body diffusion which laterally surrounds at least part of said source diffusion, a p-type buried body diffusion which underlies said channel and at least part of said surface body diffusion; an ohmic connection between said buried body diffusion and said source metallization; and a further p+ diffusion which is self-aligned to said source metallization within an aperture in said gate structure, as recited in claim 15. Note also that the drawings are objected to, above, as not illustrating every element of this claim.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7725 for regular communications and 703-308-7725 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TLD
10/2002